

**Amendment and Response**

Applicant: Steven L. Pline et al.

Serial No.: 10/725,855

Filed: December 2, 2003

Docket No.: 10014281-1

Title: DATA STORAGE SYSTEM WITH ERROR CORRECTION CODE AND REPLACEABLE DEFECTIVE MEMORY

**REMARKS**

The following remarks are made in response to the Office Action mailed May 15, 2006. Claims 1-35 were rejected. With this Response, claims 1, 2, 13-16, 18, 19, 23, 28, and 29 have been amended. Claims 1-35 remain pending in the application and are presented for reconsideration and allowance.

**U.S. Patent No. 6,119,245**

Applicants request that cited patent reference U.S. Patent No. 6,119,245 be added to the listing of references in Form PTO-892.

**Claim Rejections under 35 U.S.C. § 102**

The Examiner rejected claims 1-8, 10, 11, 13-17, 23, and 26-35 under 35 U.S.C. § 102(b) as being unpatentable over Hiratsuka, U.S. Patent No. 6,119,245 ("Hiratsuka").

Applicants submit that Hiratsuka fails to teach or suggest the invention recited by amended independent claim 1. Hiratsuka fails to teach or suggest a **data storage and retrieval system operating on a host computer, the sparing system comprising computer readable instructions stored in a host memory of the host computer and the error correction code system comprising computer readable instructions stored in the host memory of the host computer.**

**Hiratsuka** discloses a semiconductor disk device 100 including a flash memory section 110, a disk controller section 120, and a microcontroller section 130. (Col. 5, lines 9-11; and Fig. 1). Disk controller section 120 includes a host interface 121 for transferring address information and/or command information or main data etc. with the outside of semiconductor disk device 100. Disk controller section 120 also includes micro CPU interface 122 for transferring address information and/or command information or control signals etc. with respect to disk controller section 120 and microcontroller section 130. (Col. 5, lines 20-27; and Fig. 1). Micro CPU 131 in microcontroller section 130 controls flash memory section 110 and disk controller section 120 in accordance with the command information and/or address information etc. that is input from outside through host interface 121 and micro CPU interface 122. (Col. 6, lines 25-29).

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Hiratsuka further discloses that ECC control section 126, on data writing, fetches write data from flash memory interface 125 and compiles ECC data, which it then sends to flash memory interface 125. Also, when data is read, it performs an operation of inputting main data and ECC data from flash memory interface 125 and detecting whether or not a data error has been generated and/or an operation of correcting main data if generation of a COR is detected. (Col. 5, lines 46-53). Data error information management table 127 stores for each sector of memory elements M(0)-M(9) the number of times of occurrence of data errors. (Col. 5, lines 54-56). Address conversion table 128 converts memory numbers in address information that is input from the external host computer into physical memory numbers and output. (Col. 6, lines 16-19).

Hiratsuka discloses a disk controller including hardware components that provide ECC encoding and decoding, data error information management, and address conversion. The disk controller includes a host interface 121 for communicating with a host computer. ~~The host computer in Hiratsuka~~ does not perform any of the error correction, data error information management, or address conversion functions. In contrast, claim 1 recites a system that operates on a *host computer*. In addition, the sparing system and the error correction code system comprise *computer readable instructions* stored in a *host memory* of the *host computer*. The sparing system and the error correction code system recited by claim 1 are not hardware based like the disk controller disclosed by Hiratsuka.

In view of the above, Applicants respectfully submit that the above rejection of independent claim 1 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 2-8, 10, and 11 further define patentably distinct independent claim 1. Accordingly, Applicants believe that these dependent claims are also allowable over the cited reference. Allowance of claims 1-8, 10, and 11 is respectfully requested.

For the same reasons as discussed above with reference to claim 1, Applicants submit that Hiratsuka also fails to teach or suggest the invention recited by amended independent claim 13 including a **host computer comprising host memory storing instructions to provide an error correction code and to replace defective memory sections of a storage device with spare memory sections of the storage device; and a host processor that executes the instructions to encode and decode data stored in the storage device with the**

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**error correction code and to replace addresses of defective memory sections with addresses of spare memory sections.**

In view of the above, Applicants respectfully submit that the above rejection of independent claim 13 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 14-17 further define patentably distinct independent claim 13. Accordingly, Applicants believe that these dependent claims are also allowable over the cited reference. Allowance of claims 13-17 is respectfully requested.

For the same reasons as discussed above with reference to claim 1, Applicants submit that Hiratsuka also fails to teach or suggest the invention recited by amended independent claim 23 including **a host computer system comprising means for correcting errors in data retrieved from a storage style memory device, the means for correcting errors comprising computer readable instructions stored in a host memory of the host computer system; and means for sparing the defective sections of memory with replacement sections of memory in the storage style memory device, the means for sparing comprising computer readable instructions stored in the host memory of the host computer system.**

In view of the above, Applicants respectfully submit that the above rejection of independent claim 23 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 26-28 further define patentably distinct independent claim 23. Accordingly, Applicants believe that these dependent claims are also allowable over the cited reference. Allowance of claims 23 and 26-28 is respectfully requested.

For the same reasons as discussed above with reference to claim 1, Applicants submit that Hiratsuka also fails to teach or suggest the invention recited by amended independent claim 29 including **providing computer-executable sparing instructions and error correction code instructions; replacing addresses for defective memory sections in a memory device with addresses for replacement memory sections in the memory device by executing the sparing instructions on the host computer; providing the addresses for the replacement memory sections to the memory device during read and write operations with the memory device by executing the sparing instructions on the host computer; encoding original data with an error correction code to write encoded data**

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into the memory device by executing the error correction code instructions on the host computer; and decoding data retrieved from a selected memory section of the memory device with the error correction code by executing the error correction code instructions on the host computer.

In view of the above, Applicants respectfully submit that the above rejection of independent claim 29 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 30-32 further define patentably distinct independent claim 29. Accordingly, Applicants believe that these dependent claims are also allowable over the cited reference. Allowance of claims 29-32 is respectfully requested.

For the same reasons as discussed above with reference to claim 1, Applicants submit that Hiratsuka also fails to teach or suggest the invention recited by independent claim 33 including providing computer-executable sparing instructions and error correction code instructions; sparing out sections of memory in the storage style memory device by executing the sparing instructions on the host computer; and encoding and decoding data stored in the storage style memory device with an error correction code by executing the error correction code instructions on the host computer.

In view of the above, Applicants respectfully submit that the above rejection of independent claim 33 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 34 and 35 further define patentably distinct independent claim 33. Accordingly, Applicants believe that these dependent claims are also allowable over the cited reference. Allowance of claims 33-35 is respectfully requested.

**Claim Rejections under 35 U.S.C. § 103**

The Examiner rejected claim 9 under 35 U.S.C. § 103(a) as being unpatentable over Hiratsuka in view of Weng et al., U.S. Patent No. 5,428,630.

Dependent claim 9 further defines patentably distinct independent claim 1. Accordingly, Applicants believe that this dependent claim is also allowable over the cited references. Allowance of claim 9 is respectfully requested.

The Examiner rejected claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Hiratsuka in view of Martyn Riley, Reed-Solomon Codes.

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Dependent claim 12 further defines patentably distinct independent claim 1. Accordingly, Applicants believe that this dependent claim is also allowable over the cited references. Allowance of claim 12 is respectfully requested.

The Examiner rejected claims 18-20 under 35 U.S.C. § 103(a) as being unpatentable over Hiratsuka in view of Tsunoda et al., U.S. Patent Application Publication No. 2003/0028733.

Dependent claims 18-20 further define patentably distinct independent claim 13. Accordingly, Applicants believe that these dependent claims are also allowable over the cited references. Allowance of claims 18-20 is respectfully requested.

The Examiner rejected claims 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Hiratsuka in view of Kleveland et al., U.S. Patent Application Publication No. 2003/0115518.

Dependent claims 21 and 22 further define patentably distinct independent claim 13. Accordingly, Applicants believe that these dependent claims are also allowable over the cited references. Allowance of claims 21 and 22 is respectfully requested.

The Examiner rejected claims 24 and 25 under 35 U.S.C. § 103(a) as being unpatentable over Hiratsuka in view of Buternowsky et al., U.S. Patent No. 5,809,090.

Dependent claims 24 and 25 further define patentably distinct independent claim 23. Accordingly, Applicants believe that these dependent claims are also allowable over the cited references. Allowance of claims 24 and 25 is respectfully requested.

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**CONCLUSION**

In view of the above, Applicants respectfully submit that pending claims 1-35 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-35 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either Phil Lyren at Telephone No. (281) 514-8236, Facsimile No. (281) 514-8332 or Steven E. Dicke at Telephone No. (612) 573-2002, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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By his attorneys,

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Date: August 15, 2006  
SED:kmh

Steven E. Dicke  
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**CERTIFICATE UNDER 37 C.F.R. 1.8:**

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via facsimile to Facsimile No. (571) 273-8300 on this 15th day of August, 2006.

By: Steven E. Dicke

Name: Steven E. Dicke